Subject:- Digital Techniques (22320)

SYLLABUS

Chapter No.	Name of Unit	Marks With Option
1	Number Systems	18
2	Logic gates and Logic families	18
3	Combinational Logic Circuits	20
4	Sequential Logic Circuits	26
5	Data Converters and PLDs	20
	Total Marks :-	**102**

BOARD THEORY PAPER PATTERN FOR DTE (22320)

Q.1		**Attempt any FIVE**	**5*2=10**
	a)	Number Systems.	
	b)	Logic gates and Logic families	
	c)	Combinational Logic Circuits	
	d)	Combinational Logic Circuits	
	e)	Sequential Logic Circuits.	
	f)	Sequential Logic Circuits.	
	g)	Sequential Logic Circuits.	
Q.2		**Attempt any THREE**	**3*4=12**
	a)	Data Converters and PLDs	
	b)	Number Systems	
	c)	Logic gates and Logic families	
	d)	Combinational Logic Circuits	
Q.3		**Attempt any THREE**	**3*4=12**
	a)	Combinational Logic Circuits	

	b)	Logic gates and Logic families
	c)	Sequential Logic Circuits.
	d)	Logic gates and Logic families
Q.4		**Attempt any FOUR** **3*4=12**
	a)	Sequential Logic Circuits.
	b)	Combinational Logic Circuits
	c)	Data Converters and PLDs
	d)	Logic gates and Logic families
	e)	Combinational Logic Circuits
Q.5		**Attempt any TWO** **2*6=12**
	a)	Number Systems
	b)	Sequential Logic Circuits.
	c)	Data Converters and PLDs
Q.6		**Attempt any TWO** **2*6=12**
	a)	Number Systems
	b)	Data Converters and PLDs
	c)	Sequential Logic Circuits.

CLASS TEST - I

PAPER PATTERN

COURSE: - Digital Techniques (22320)
PROGRAMME: - Computer Technology

Syllabus :-

Unit No.	Name of the Unit	Course Outcome (CO)
1	Number Systems	CO-320.1
2	Logic gates and Logic families	CO-320.2
3	Combinational Logic Circuits	CO-320.3

Q.1	Attempt any FOUR4*2=8Marks	Course Outcome (CO)
a)	Number Systems	CO-320.1
b)	Logic gates and Logic families	CO-320.2
c)	Logic gates and Logic families	CO-320.2
d)	Logic gates and Logic families	CO-320.2
e)	Combinational Logic Circuits	CO-320.3
f)	Number System	CO-320.1
Q.2	Attempt any THREE3*4=12 Marks	
a)	Number System	CO-320.1
b)	Logic gates and Logic families	CO-320.2
c)	Combinational Logic Circuits	CO-320.3
d)	Logic gates and Logic families	CO-320.2
e)	Logic gates and Logic families	CO-320.2
f)	Combinational Logic Circuits	CO-320.3

CLASS TEST - II

PAPER PATTERN

COURSE: - Digital Techniques (22320)
PROGRAMME: Computer Technology

Syllabus :-

Unit	Name of the Unit	Course Outcome(CO)
3	Combinational Logic Circuits	CO-320.3
4	Sequential Logic Circuits	CO-320.4
5	Data Converters and PLDs	CO-320.5

Q.1	Attempt any FOUR 4*2=8Marks	Course Outcome (CO)
a)	Combinational Logic Circuits	CO-320.3
b)	Sequential Logic Circuits	CO-320.4
c)	Combinational Logic Circuits	CO-320.3
d)	Sequential Logic Circuits	CO-320.4
e)	Data Converters and PLDs	CO-320.5
f)	Data Converters and PLDs	CO-320.5
Q.2	Attempt any THREE 3*4=12 Marks	
a)	Combinational Logic Circuits	CO-320.3
b)	Sequential Logic Circuits	CO-320.4
c)	Sequential Logic Circuits	CO-320.4
d)	Data Converters and PLDs	CO-320.5
e)	Combinational Logic Circuits	CO-320.3
f)	Combinational Logic Circuits	CO-320.3

COURSE OUTCOME (CO)

COURSE: - Digital Technique (22320)

PROGRAMME: - Computer Technology

CO.NO	Course Outcome
CO-320.1	Use number system and codes for interpreting working of digital system
CO-320.2	Use Boolean expressions to realize logic circuits.
CO-320.3	Build simple combinational circuits.
CO-320.4	Build simple Sequential circuits.
CO-320.5	Test data converters and PLDs in digital electronics system.

1. Number System

Position in Question Paper **Total Marks-18**

Q.1. a) 2-Marks.
Q.2. b) 4-Marks.
Q.5. a) 6-Marks.
Q.6. a) 6-Marks.

Descriptive Question

1. Convert (57) into binary equivalent. 02) Convert (268.75)10 = (?)2
2. Convert (420) 10 = (?)2
3. Find BCD code for following decimal number. 1.39 2. 47
4. Perform BCD addition for (2375)+(4933)
5. Write the radix of Binary , octal, decimal and hexadecimal number system
6. List the binary , octal and hexadecimal numbers for decimal no. 0 to 15.
7. Convert 1. (1101.0011)-------- (?)16
   2. (00010001)------(?)8
8. Add (83)10 and (34)10 in BCD
9. Perform the BCD arithmetic:
   1. (264)10+ (668)10
   2. (454)10 + (379)10
10. Convert 1. (255)10= (?)16 = (?)8
    2. (157)10= (?)BCD = (?) Excess 3_
11. Perform 2's complement subtraction (59)10 - (62)10

MCQ Questions:-

(Total number of Question=Marks*3=8*3=24)

Note: Correct answer is marked with **bold.**

1. The Base of Binary no.system is...
   - **a) 2**
   - c)10
   - b) 8
   - d 16
2. Convert the following binary number to decimal. (01010)
   - a)11
   - c)15
   - b)35
   - **d)10**
3. The Binary Addition of 1+1 is
   - a) 0 with 0 Carry
   - c) 1 with carry 0
   - **b) 0 with Carry 1**
   - d) 1 with carry 0
4. Convert (214)8 into decimal
   - a) (140)10
   - **c)(142)10**
   - b) (141)10
   - d)(130)10
5. Convert binary to octal: (110110001010)2
   - a) (5512)8
   - c)(4532)8
   - **b) (6612)8**
   - d)(130)10
6. The decimal equivalent of the binary number (1011.011)2 is _____
   - a) (11.375)10
   - **c)(11.175)10**
   - b) (10.123)10
   - d)(9.23)10
7. Binary coded decimal is a combination of _____
   - a) 2 binary digits
   - **c)4 binary digits**
   - b) 3s binary digits
   - d)5 binary digits
8. The given hexadecimal number (1E.53)16 is equivalent to _____
   - a) (35.684)8
   - c) (34.340)8
   - **b) (36.246)8**
   - d) (35.599)8
9. The octal number (651.124)8 is equivalent to _____
   - **a) (1A9.2A)16**
   - c) (1A8.A3)16
   - b) (1B0.10)16
   - d) (1B0.B0)16
10. The octal equivalent of the decimal number (417)10 is _____
    - **a) (641)8**
    - c) (640)8
    - b) (619)8
    - d) (598)8

11. Convert the hexadecimal number (1E2)16 to decimal:
a) 480 **c) 482**
b) 483 d) 484

12. (170)10 is equivalent to
a) (FD)16 **c) (AA)16**
b) (DF)16 d) (AF)16

13. Convert (214)8 into decimal:
a) (140)10 c) (142)10
b) (141)10 d) (130)10

14. Convert (0.345)10 into an octal number:
a) (0.16050)8 c) (0.19450)8
b) (0.26050)8 d) (0.24040)8

15. Convert the binary number (01011.1011)2 into decimal:
a) (11.6875)10 c) (10.9876)10
b) (11.5874)10 d) (10.7893)10

16. Octal to binary conversion: (24)8 =?
a) (111101)2 c) (111100)2
b) (010100)2 d) (101010)2

17. Convert binary to octal: (110110001010)2 =?
a) (5512)8 c) (4532)8
b) (6612)8 d) (6745)8

18. Any signed negative binary number is recognized by its _____
a) MSB c) Byte
b) LSB d) Nibble

19. The parameter through which 16 distinct values can be represented is known as _____
a) Bit **c) Word**
b) Byte d) Nibble

20. If the decimal number is a fraction then its binary equivalent is obtained by _____ the number continuously by 2.
a) Dividing c) Adding
b) Multiplying d) Subtracting

21. The representation of octal number (532.2)8 in decimal is _____
a) (346.25)10 c) (340.67)10
b) (532.864)10 d) (531.668)10

22. The decimal equivalent of the binary number (1011.011)2 is _____

a) (11.375)10 c) (11.175)10
b) (10.123)10 d) (9.23)10

23. The decimal equivalent of the octal number (645)8 is _____
a) (450)10 **c) (421)10**
b) (451)10 d) (501)10

24. The largest two digit hexadecimal number is _____
a) (FE)16 **c) (FF)16**
b) (FD)16 d) (EF)16

25. The quantity of double word is _____
a) 16 bits c) 4 bits
b) 32 bits d) 8 bits

26. The binary number 11011 is equivalent to decimal number
a)19 **c) 27**
b)12 d) 21

27. The largest two-digit hexadecimal number is
a) FE c)EF
b) FD **d) FF**

28. A Nibble is equal to _____ bit(s).
a) 1 **c) 4**
b) 2 d) 8

29.1 Kilobits are equal to___
a) 1000 bits c) 1012 bits
b)1024 bits d) 1008 bits

2. Logic gates and Logic Families

Position in Question Paper **Total Marks-18**

Q.1. b) 2-Marks.
Q.2. c) 4-Marks.
Q.3. b) 4-Marks.
Q.3. d) 4-Marks.
Q.4. d) 4-Marks.

Descriptive Question

1. State any two Boolean laws with expression
2. Define duality theorem .Give example
3. Draw the symbol and truth table of NOT and OR gate.
4. Draw the symbol and truth table of NOR gate.
5. Draw the symbol and truth table of NOR gate.
6. Why NAND and NOR gates are called as universal gate?
7. Define 1. Fan in 2. Fan out
8. Define 1. Fan in 2) Noise immunity.
9. State any two Boolean laws with expression
10. State and prove De Morgan's theorems.
11. State and explain duality theorems.
12. Draw the logic symbol and truth table of NAND and NOR gate.
13. Derive NOT gate and AND gate using NOR gate only.
14. Draw X-OR gate using NAND gate only. Also write output of each gate.
15. Design logic circuit for following expression using universal gates:
    Y= (A+B) (A+C)
16. Compare CMOS and TTL logic families.

MCQ Question

(Total number of Question=Marks*3=12*3=36)

Note: Correct answer is marked with **bold**

1. The expression for Absorption law is given by _____
   a) A + AB = A
   c) AB + AA' = A
   b) A + AB = B
   d) A + B = B + A
2. According to boolean law: A + 1 = ?
   a)1
   c) 0
   b)A
   d) A'
3. DeMorgan's theorem states that _____
   a) (AB)' = A' + B'
   c) A' + B' = A'B'
   b) (A + B)' = A' * B
   d)(AB)' = A' + B
4. In boolean algebra, the OR operation is performed by which properties?
   a) Associative properties
   c) Distributive properties
   b)Commutative properties
   d**) All of above**
5. How many AND gates are required to realize Y = CD + EF + G
   a)4
   c)3
   b)5
   d)2
6. The NOR gate output will be high if the two inputs are
   a) 00
   c)10
   b) 01
   d)11
7. Universal gates are _____
   a) NAND & NOR
   c) XOR & OR
   b) AND & OR
   d) EX-NOR & XOR
8. How many AND gates are required to realize Y = CD + EF + G?
   a)4
   c)3
   b) 5
   d) 2
9. The NOR gate output will be high if the two inputs are _____
   a) 00
   c) 10
   b) 01
   d) 11
10. The NOR gate output will be high if the two inputs are _____

a) 00 c) 10
b) 01 d) 11

11. How many two input AND gates and two input OR gates are required to realize Y = BD + CE + AB?
a) 3, 2 c) 1, 1
b) 4, 2 d) 2, 3

12. Which of the following are known as universal gates?
a) NAND & NOR c) XOR & OR
b) AND & OR d) EX-NOR & XOR

13. The gates required to build a half adder are _____
a) EX-OR gate and NOR gate c) EX_OR gate and AND gate
b) EX-OR gate and OR gate d) EX-NOR gate and AND gate

14. The inverter is ……
a) NOT gate c) AND gate
b) OR gate d) None of the above

15. The inputs of a NAND gate are connected together. The resulting circuit is …….
a) OR gate **c) NOT gate**
b) AND gate d) None of the above

16. The NOR gate is OR gate followed by ……
a) AND gate **c) NOT gate**
b) NAND gate d) None of the above

17. The NAND gate is AND gate followed by ……
a) NOT gate c) AND gate
b) OR gate d) None of the above

18. Digital circuit can be made by the repeated use of ……
a) OR gates **c) NAND gates**
b) NOT gates d) None of the above

19. The only function of NOT gate is to ……..
a) Stop signal c) Act as a universal gate
b) Invert input signal d) None of the above

20. When an input signal 1 is applied to a NOT gate, the output is ……
a) 0 c) Either 0 & 1
b) 1 d) None of the above

21. In Boolean algebra, the bar sign (-) indicates ……..
a) OR operation c)NOT operation
b) AND operation d) None of the above

22. An OR gate has 4 inputs. One input is high and the other three are low.

The output is …….

a) Low

b) **High**

c) alternately high and low

d))may be high or low depending on reative magnitude of inputs

23. Both OR and AND gates can have only two inputs.

a) True **b) False**

24. The output will be a LOW for any case when one or more inputs are zero in a/an ……

a) OR Gate **c) AND Gate**

b) NOT Gate d) NAND Gate

25. ……. NAND circuits are contained in a 7400 NAND IC.

a) 1 **c) 4**

b) 2 d) 8

26. Exclusive-OR (XOR) logic gates can be constructed from ……..logic gates.

a) OR gates only **c) AND gates, OR gates, and NOT gates**

b) AND gates and NOT gates d) OR gates and NOT gates

27. …….. truth table entries are necessary for a four-input circuit.

a) 4 c)12

b) 8 **d)16**

28. A NAND gate has …….. inputs and ……. output.

a) LOW inputs and LOW outputs

b) HIGH inputs and HIGH outputs

c)Low inputs and high outputs

d) None of the above

29. The basic logic gate whose output is the complement of the input is …….

a) OR gate **c) INVERTER gate**

b) AND gate d) Comparator

30. …….. input values will cause an AND logic gate to produce a HIGH output.

a) At least one input is HIGH **c)All inputs are HIGH**

b)At least one input is LOW d) All inputs are LOW

31. …….. input values will cause an AND logic gate to produce a HIGH output.

a) At least one input is HIGH **c)All inputs are HIGH**

b) At least one input is LOW d) All inputs are LOW

32. The basic logic gate whose output is the complement of the input is …….

a) OR gate **c)INVERTER gate**

b) AND gate d)Comparator

33. A NAND gate has …….. inputs and ……. output.
a) LOW inputs and LOW outputs
b) HIGH inputs and HIGH outputs
c)**low inputs and high outputs**
d)none of the above

34. …….. truth table entries are necessary for a four-input circuit.
a) 4
b) 8
c) 12
d) 16

35. Exclusive-OR (XOR) logic gates can be constructed from ……..logic gates.
a) OR gates only
b) AND gates and NOT gates
c)AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

36. ……. NAND circuits are contained in a 7400 NAND IC.
a) 1
b) 2
c) 4
d) 8

3. Combinational Logic Circuits

Position in Question Paper **Total Marks-20**

Q.1. c) 2-Marks.
Q.1. d) 2-Marks.
Q.2. d) 4-Marks.
Q.3. a) 4-Marks.
Q.4. b) 4-Marks.
Q.4. e) 4-Marks

Descriptive Question

1. Explain the concept of minterm and maxterm.
2. Differentiate between combinational circuits & Sequential circuits.
3. Convert standard SOP expression into canonical SOP: Y= A+BCD
4. Draw K-Map for Y=∑m(0,1,2,4,5,6) and simplify.
5. Draw the block diagram of 1:4 Demultiplexer and write its truth table.
6. Draw the block diagram of BCD to 7 Segment decoder.
7. Convert the following expression into its canonical form-

   $Y=(A+B)\ (B+\overline{C})(A+\overline{C})$
8. Realize the following expression using Multiplexer

   Y=∑m (1,4,6,8,11,14,15)
9. Minimize the expression using K-map
   Y=∑m (0,2,4,5,13,14,15)
10. Design 8:1 MUX using 4:1 MUX
11. Design full adder using k-map and draw logic diagram
12. Design half adder using K-Map.
13. Design 8:1 using 4:1 MUX

MCQ Questions:-

(Total number of Question=Marks*3= 18*3=54)

Note: Correct answer is marked with **bold.**

1.A full adder logic circuit will have _____

a) Two inputs and one output
c) Two inputs and two outputs
b) Three inputs and three outputs
d)Three inputs and two outputs

2. The gates required to build a half adder are _____

a) EX-OR gate and NOR gate
c)EX-OR gate and AND gate
b) EX-OR gate and OR gate
d) EX-NOR gate and AND gate

3. There are _____ cells in a 4-variable K-map.

a) 12
c) 18
b) 16
d) 8

4. Don't care conditions can be used for simplifying Boolean expressions in _____

a) Registers
c) K-maps
b) Terms
d) Latches

5. No. of Inputs available for Half Substractors are_____

a) 1
c) 3
b) 2
d) 4

6. No.of Outputs of Full Adders are _____

a) 1
c) 3
b) 2
d) 4

7. Multiplexer is a___

a) Type of decoder which decodes several inputs and gives one output
b) Device which converts many signals into one
c) Takes one input and results into many output
d) Type of encoder which decodes several inputs and gives one output

8. The function of an enable input on a multiplexer chip is___

a) To apply Vcc
c) To active the entire chip
b) To connect ground
d) To active one half of the chip

9.Number of select lines would be required for an 8-line-to-1-line multiplexer?

a) 2
c) 8
b) 4
d) 3

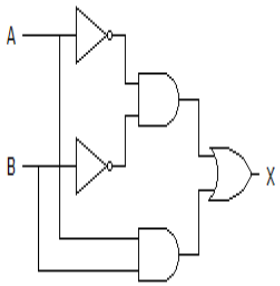
10. The word demultiplexer means _____

a) One into many
c) both a & b
b) Many into one
d) One into one

11. In 1-to-4 demultiplexer, how many select lines are required ?

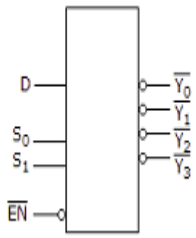
a) 2
c) 1
b) 3
d) 4

12. Which of the following logic expressions represents the logic diagram shown?



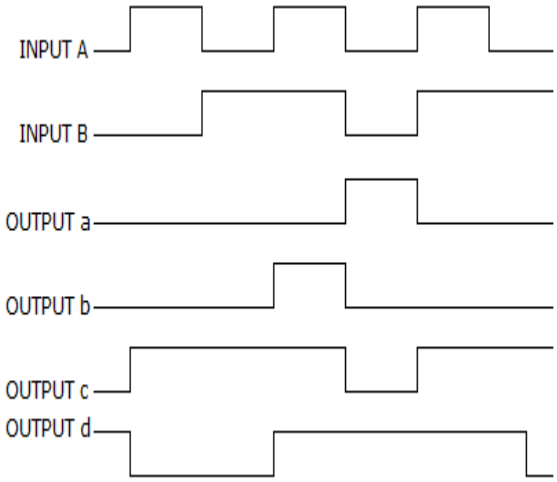
a) X=AB'+A'B
c) X=(AB)'+A'B'
b) X=(AB)'+AB
d) X=A'B'+AB

13. The device shown here is most likely a _____



a)XOR
c) AND
b) XNOR
d) XAND

14. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



a) d
b) a
c)c
d)b

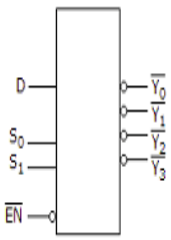
16. Which of the following combinations of logic gates can decode binary 1101?

a) One 4-input AND gate
b) One 4-input AND gate, one inverter
c) One 4-input NOT gate
d) One 4-input NAND gate.

17. What is the indication of a short to ground in the output of a driving gate?

a) Only the output of the defective gate is affected
b) There is a signal loss to all load gates
c) The node may be stuck in either the HIGH or the LOW state
d) The affected node will be stuck in the HIGH state

18. For the device shown here, assume the D input is LOW, both S inputs are LOW and the input is LOW. What is the status of the Y' outputs?



a) All are HIGH
b) All are LOW
c) All but Y0 are LOW
d) All but Y0 are HIGH

19. The carry propagation can be expressed as _____

a) Cp = AB
b) Cp = A + B
c) All but Y0 are LOW
d) All but Y0 are HIGH

21. 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

22. The basic building blocks of the arithmetic unit in a digital computers are _____
a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

23. A digital system consists of _____ types of circuits.
a) 2
b) 3
c) 4
d) 5

24. In a combinational circuit, the output at any time depends only on the _____ at that time.
a) Voltage
b) Intermediate values
c) Input values
d) Clock puls

25. In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values
b) Intermediate values
c) Both past output and present input
d) Present input values

26. Procedure for the design of combinational circuits are:

A .From the word description of the problem, identify the inputs and outputs and draw a block diagram.
B. Draw the truth table such that it completely describes the operation of the circuit for different combination of inputs
C. Simplify the switching expression(s) for the output(s).
D. Implement the simplified expression using logic gates.
E. Write down the switching expression(s) for the output(s).

a) B, C, D, E, A
b) A, D, E, B, C
c) A, B, E, C, D
d) B, A, E, C, D

27. All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) NAND and NOR operations

28. The design of an ALU is based on _____
a) Sequential logic
c) Multiplexing

b) Combinational logic d) De-Multiplexing

29. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.
a) Input, zero c) Input, one
b) Output, one **d) Output, zero**

30. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
a) An underflow condition **c) An overflow condition**
b) A neutral condition d) One indication

31. The flag bits in an ALU is defined as _____
a) The total number of registers c) The total number of control lines
b) The status bit conditions d) All of the Mentioned

32. A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay **c) Rotary switch**
b) DPDT switch d) Linear stepper

33. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3 **c) 2**
b) 4 d) 5

34.The enable input is also known as _____
a) Select input **c) Strobe**
b) Decoded input d) Sink

35. BCD adder can be constructed with 3 IC packages each of _____
a) 2 bits **c) 4 bits**
b) 3 bits d) 5 bits

36.In which of the following gates, the output is 1, if and only if at least one input is 1?
a)NOR **c)OR**
b)AND d)NAND

37. The time required for a gate or inverter to change its state is called
a)Rise time **c)Propagation time**
b)Decay time d)Charging time

38. The time required for a pulse to change from 10 to 90 percent of its maximum value is called
a)Rise time c)Propagation time
b)Decay time d)Operating speed

39. The maximum frequency at which digital data can be applied to gate is called
a)Operating speed c).Binary level transaction period

b)Propagation speed d).Charging time

40. What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?
a)one **c)three**
b)two d)four

41. Odd parity of word can be conveniently tested by
a)OR gate c)NOR gate
b)AND gate **d)XOR gate**

42. Which one of the following will give the sum of full adders as output ?
a)Three point majority circuit
b)Three bit parity checker
c)Three bit comparator
d)Three bit counter

43. The time required for a pulse to decrease from 90 to 10 per cent of its maximum value is called The time required for a pulse to decrease from 90 to 10 per cent of its maximum value is called
a)Decay time c)n period
b)Binary level transitio d)propagation delay

44. Which of the following gates would output 1 when one input is 1 and other input is 0 ?
a)OR gate c)NAND gate
b)AND gate **d)both (a) and ©**

45 Which of the following expressions is not equivalent to X ' ?
a)X NAND X c)X NAND 1
b)X NOR X d)X NOR 1

46. Which of the following gates are added to the inputs of the OR gate to convert it to the NAND gate ?
a)NOT c)OR
b)AND d)XOR

47. The EXCLUSIVE NOR gate is equivalent to which gate followed by an inverter ?
a)OR c)NAND
b)AND **d)XOR**

48. A one-to-four line demultiplexer is to be implemented using a memory. How many bits must each word have ?
a)1 bit c)4 bits
b)2 bits d)8 bits

49. What logic function is produced by adding an inverter to the output of an AND gate ?
a)NAND c)XOR

b)NOR d)OR

50. Which of the following gates is known as coincidence detector ?

a)AND gate c)NOT gate

b)**OR gate** **d)NAND gate**

51. Which table shows the logical state of a digital circuit output for every possible combination of logical states in the inputs ?

a)Function table c)Routing table

b)Truth table d)ASCII table

52. A positive AND gate is also a negative

a)NAND gate c)AND gate

b)NOR gate **d)OR gate**

53. An OR gate can be imagined as

a)Switches connected in series c)MOS transistors connected in series

b)Switches connected in parallel d)None of these

54. Which combination of gates does not allow the implementation of an arbitrary boolean function?

a)OR gates and AND gates only c)OR gates and NOT gates only

b)OR gates and exclusive OR gate d)NAND gates only

4. Sequential logic Circuits.

Position in Question Paper **Total Marks-26**

Q.1. e) 2-Marks.
Q.1. f) 2-Marks.
Q.1. g) 2-Marks.
Q.3. c) 4-Marks.
Q.4. a) 4-Marks.
Q.5. b) 6-Marks
Q.6. c) 6-Marks

Descriptive Questions

1. What is clock? What is its use?
2. Draw RS latch using NAND gate only.
3. What are the various methods of triggering a flip flop?
4. What is the difference between edge triggering and level triggering?
5. Draw the ckt. of SR flip flop using NAND gate.
6. Draw logic symbol and truth table of D- F/F.
7. Draw logic symbol and truth table of JK- F/F.
8. Derive excitation table of D F/F.
9. Explain different triggering methods used in flip flop.
10. Describe the operation of RS flip flop using NAND gate only.
11. Describe the function of preset and clear terminals in JK F/F.
12. Convert JK flip flop into T F/F write its truth table.
13. State different applications of F/Fs.
14. Draw the block diagram of SISO shift register and explain it.
15. Draw and describe universal Shift Register.
16. Design MOD-10(Decade) counter using T F/Fs.

MCQ Questions:-

(Total number of Question=Marks*3= 18*3=54)

Note: Correct answer is marked with **bold.**

1.Latch is a device with _____
a) One stable state
c) Three stable state
b) Two stable state
d) Infinite stable states

2. The full form of SR is _____
a) System rated
c) Set ready
b) Set Reset
d) Set Rated

3. The inputs of SR latch are _____
a) X and Y
c) S and R
b) A and B
d) J and K

4. The difference between a flip-flop & latch is _____
a) Both are same
b) Flip-flop consist of an extra output
c) Latches has one input but flip-flop has two
d) Latch has two inputs but flip-flop has one

5. The S-R flip flop consist of _____
a) 4 AND gates
c) An additional clock input
b) Two additional AND gates
d) 3 AND gates

6.The characteristic of J-K flip-flop is similar to _____
a) S-R flip-flop
c) T flip-flop
b) D flip-flop
d) Gated T flip-flop

7. J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting ____
a) Two AND gates
c) Two NOT gates
b) Two NAND gates
d) Two OR gate

8. On a J-K flip-flop, when is the flip-flop in a hold condition?
a) J= 0, K = 0
c) J = 0, K = 1
b) J = 1, K = 0
d) J = 1, K = 1

9. The D flip-flop has _____ input
a) 1
c) 3
b) 2
d) 4

10. D flip-flop has _____ output/outputs.
a) 2
c) 4

b) 3 d) 1

11. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages c) Gate impedance
b) Synchronous operation **d) Cross coupling**

12. One example of the use of an S-R flip-flop is as _____
a) Transition pulse generator
b) Racer **c) Switch debouncer**

13. The truth table for an S-R flip-flop has how many VALID entries?
a) 1 **c) 3**
b) 2 d) 4

14. When both inputs of a J-K flip-flop cycle, the output will _____
a) Be invalid **c) Not change**
b) Change d) Toggle

15. Which of the following is correct for a gated D-type flip-flop?
a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW
b) The output complement follows the input when enabled
c) Only one of the inputs can be HIGH at a time
d) The output toggles if one of the inputs is held HIGH

16. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates **c) NOR or NAND gates**
b) XOR or XNOR gates d) AND or NOR gates

17.The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
a) Combinational circuits c) Latches
b) Sequential circuits d) Flip-flop

18. Whose operations are more faster among the following?
a) Combinational circuits c) Latches
b) Sequential circuits d) Flip-flops

19. How many types of sequential circuits are?
a) 2 c) 4
b) 3 d) 5

20. In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set c)Previous state
b) Reset d)Current state

21. The D flip-flop has _____ input
a) 1 c) 3
b) 2 d) 4

22 . A D flip-flop can be constructed from an _____ flip-flop.
a) S-R c)T
b) J-K d)S-K

23. In J-K flip-flop, the function K=J is used to realize _____
a) D flip-flop **c) T flip-flop**
b) S-R flip-flop d) S-K flip-flop

24. The only difference between a combinational circuit and a flip-flop is that
a) The flip-flop requires previous state
b) The flip-flop requires next state
c).The flip-flop requires a clock
d) The flip-flop depends on the past as well as present states

25. The flip-flop is only activated by _____
a) Positive edge trigger
b) Negative edge trigger
c) Either positive or Negative edge trigger
d) Sinusoidal trigger

26. In D flip-flop, if clock input is HIGH & D=1, then output is _____
a) 0 c) Forbidden
b) 1 d) Toggle

27. The characteristic equation of J-K flip-flop is _____
a) Q(n+1)=JQ(n)+K’Q(n) c) Q(n+1)=JQ'(n)+KQ(n)
b) Q(n+1)=J’Q(n)+KQ'(n) **d) Q(n+1)=JQ'(n)+K’Q(n)**

28. In D flip-flop, D stands for _____
a) Distant c) Desired
b) Data d) Delay

29. What does the circle on the clock input of a J-K flip-flop mean?
a) Level enabled **c) negative edge triggered**
b) Positive edge triggered d) Level triggered

30 . What does the direct line on the clock input of a J-K flip-flop mean?
a) Level enabled c) negative edge triggered
b) Positive edge triggered **d) Level triggered**

31. What does the triangle on the clock input of a J-K flip-flop mean?
a) Level enabled c) Both Level enabled
b) Edge triggered d) Level triggered

32.Both the J-K & the T flip-flop are derived from the basic _____
a) S-R flip-flop
c) D latch
b) S-R latch
d) D flip-flop

33.The S-R latch composed of NAND gates is called an active low circuit because _____
a) It is only activated by a positive level trigger
b) It is only activated by a negative level trigger
c) It is only activated by either a positive or negative level trigger
d) It is only activated by sinusoidal trigger

34.How many stable states combinational circuits have?
a) 3
c) 2
b) 4
d) 5

35. With regard to a D latch _____
a) The Q output follows the D input when EN is LOW
b) The Q output is opposite the D input when EN is LOW
c) The Q output follows the D input when EN is HIGH
d) The Q output is HIGH regardless of EN's input state

36. Which of the following is correct for a D latch?
a) The output toggles if one of the inputs is held HIGH
b) Q output follows the input D when the enable is HIGH
c) Only one of the inputs can be HIGH at a time
d) The output complement follows the input when enabled

37. Which of the following describes the operation of a positive edge-triggered D flip-flop?
a) If both inputs are HIGH, the output will toggle
b) The output will follow the input on the leading edge of the clock
c)When both inputs are LOW, an invalid state exists
d) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock

38. A positive edge-triggered D flip-flop will store a 1 when _____
a) The D input is HIGH and the clock transitions from HIGH to LOW
b) The D input is HIGH and the clock transitions from LOW to HIGH
c) The D input is HIGH and the clock is LOW
d) The D input is HIGH and the clock is HIGH

39.The outputs of SR latch are _____
a) x and y
c) s and r
b) a and b
d) q and q'

40.The SR latch consists of _____
a) 1 input
c) 3 inputs
b) 2 inputs
d) 4 inputs

41.The NAND latch works when both inputs are _____
a) 1
c) Inverted
b) 0
d) Don't cares

42.The first step of the analysis procedure of SR latch is to _____
a) label inputs
c) label states
b) label outputs
d) label tables

43. When both inputs of SR latches are low, the latch _____
a) Q output goes high
b) Q' output goes high
c) It remains in its previously set or reset state
d) it goes to its next set or reset state

44. When both inputs of SR latches are high, the latch goes _____
a) Unstable
c) Metastable
b) Stable
d) Bistable

45. When a high is applied to the Set line of an SR latch, then _____
a) Q output goes high
c) Q output goes low
b) Q' output goes high
d) Both Q and Q' go high

46. The full form of SR is _____
a) System rated
c) Set ready
b) Set reset
d) Set Rated

47. How many types of latches are _____
a) 4
c) 2
b) 3
d) 5

48. Two stable states of latches are _____
a) Astable & Monostable
c) High output & low output
b) Low input & high output
d) Low output & high input

49. Why latches are called memory devices?
a) It has capability to stare 8 bits of data
c) It can store one bit of data
b) It has internal memory of 4 bit
d) It can store amount of data

50. Latch is a device with _____
a) One stable state
c) Three stable state
b) Two stable state
d) Infinite stable states

51. A latch is an example of a _____

a) Monostable multivibrator
c) Bistable multivibrator
b) Astable multivibrator
d) 555 timer

52. What is an ambiguous condition in a NAND based S'-R' latch?
a) S'=0, R'=1
c) S'=1, R'=1
b) S'=1, R'=0
d) S'=0, R'=0

53. A NAND based S'-R' latch can be converted into S-R latch by placing _____
a) A D latch at each of its input
b) An inverter at each of its input
c) It can never be converted
d) Both a D latch and an inverter at its input

54. The characteristic equation of S-R latch is _____
a) Q(n+1) = (S + Q(n))R'
c) Q(n+1) = S'R + Q(n)R
b) Q(n+1) = SR + Q(n)R
d) Q(n+1) = S'R + Q'(n)R

5. Data Converters and PLDs.

Position in Question Paper **Total Marks-20**

Q.2. a) 4-Marks.
Q.4. c) 4-Marks.
Q.5. c) 6-Marks.
Q.6. b) 6-Marks.

Descriptive Questions

1. State the necessity of A/D and D/A Converter.
2. List the applications of DAC
3. Define Resolution and settling time.
4. Define any two specifications of DAC
5. Define conversion time and Resolution.
6. Give any two applications of ADC.
7. State different types of memories.
8. Compare RAM and ROM.
9. Explain R-2R ladder network. Describe it in brief.
10. Compare R-2R and weighted resistor DAC
11. Explain any four Specifications of DAC
12. With Suitable diagram explain working of Ramp type ADC.
13. Draw and explain Successive approximation type ADC.
14. Describe the operation of RS flip flop using NAND gate only.
15. State any Four specifications of ADC.

MCQ Questions:-

(Total number of Question=Marks*3= 14*3=42)

Note: Correct answer is marked with **bold.**

1._____ ADC has a fixed conversion time.

a) Counter comparator ADC
c) Double ramp ADC
b) Wilkinson ADC
d) Successive approximation ADC

2. The R-2R ladder DAC has the drawback____

a) Higher values of resistance are required
c) Non-linearity due to power dissipation
b) Lesser word length
d) None of the above

3. Resolution of a 6 bit DAC can be stated as__

a) Resolution of 1 part in 63
c) Resolution of 1.568% of full scale
b) 6-bit resolution
d) All of the mentioned

4. The resolution of a 0–5 V 6-bit digital-to-analog converter (DAC) is

a) 63 %
c) 1.56 %
b) 64 %
d) 15.6%

5.Settling time for DAC 0808 is

a) 20msec
c) 100nsec
b) 50nsec
d) 150nsec

6. Conversion time of ADC 0809 is

a) 50us
c) 100us
b) 75us
d) 20ms

7. Widely used ADC are

a) ADC0809
c) ADC 0805
b) ADC 0806
d) ADC0808

8. Widely used DAC are

a) DAC0808
c) DAC0805
b) DAC0804
d) DAC0807

9. How many control lines are present in analog to digital converter in addition to reference voltage?

a) Three
c) One
b) Two
d) None of the mentioned

10. Find out the integrating type analog to digital converter?

a) Flash type converter
c) Counter type converter
b)Tracking converter
d) Dual slope ADC

11. Which type of ADC follow the conversion technique of changing the analog input signal to a linear function of frequency?
a) Direct type ADC
c) Both integrating & direct type ADC
b) Integrating type ADC
d) None of the mentioned

12. Which A/D converter is considered to be simplest, fastest and most expensive?
a) Servo converter
c) Flash type ADC
b) Counter type ADC
d) All of the mentioned

13. Drawback of counter type A/D converter
a) Counter clears automatically
c) High conversion time
b) More complex
d) Low speed

14. How to overcome the drawback of the charge balancing ADC?
a) By using precision integrator
c) By using voltage comparator
b) By using Voltage to frequency converter
d) By using dual slope converter

15. The first step in the design of memory decoder is _____
a) Selection of a EPROM
c) Address assignment
b) Selection of a RAM
d) Data insertion

16. How many address bits are required to select memory location in the Memory decoder?
a) 4 KB
c) 12 KB
b) 8 KB
d) 16 KB

17. IC 4116 is organised as _____
a) 512 * 4
c) 32 * 4
b) 16 * 1
d) 64 * 2

18. PLD contains a large number of _____
a) Flip-flops
c) Registers
b) Gates
d) All of the Mentioned

19. Logic circuits can also be designed using _____
a) RAM
c) PLD
b) ROM
d) PLA

20. In PLD, there are provisions to perform interconnections of the gates internally, because of _____
a) High reliability
c) The desired logic implementation
b) High conductivity
d) The desired output

21. How many types of PLD is?
    a) 2
    b) 3
    c) 4
    d) 5
22. How many types of PLD is?
    a) 2
    c) 4
    b) 3
    d) 5
23. The full form of PLD is _____
    a) Programmable Load Devices
    b) Programmable Logic Data
    c) Programmable Logic Devices
    d) Programmable Loaded Devices
24. The inputs in the PLD is given through _____
    a) NAND gates
    b) OR gates
    c) NOR gates
    d) AND gates
25. PAL refers to _____
    a) Programmable Array Loaded
    b) Programmable Logic Array
    c) Programmable Array Logic
    d) Programmable AND Logic
26. Outputs of the AND gate in PLD is known as _____
    a) Input lines
    b) Output lines
    c) Strobe lines
    d) Control lines
27. PLA contains _____
    a) AND and OR arrays
    b) NAND and OR arrays
    c) NOT and AND arrays
    d) NOR and OR arrays
28. PLA is used to implement _____
    a) A complex sequential circuit
    b) A simple sequential circuit
    c) A complex combinational circuit
    d) A simple combinational circuit
29. For programmable logic functions, which type of PLD should be used?
    a) PLA
    b) PAL
    c) CPLD
    d) SLD
30. The difference between a PAL & a PLA is _____
    a) PALs and PLAs are the same.
    b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
    c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
    d) The PAL has more possible product terms than the PLA
31. If a PAL has been programmed once _____
    a) Its logic capacity is lost
    c) Its outputs are only active LOW

b) Its outputs are only active.
d) It cant be reprogrammed.

32. The FPGA refers to _____
a) First programmable Gate Array
c) First Program Gate Array
b) Field Programmable Gate Array
d) Field Program Gate Array

33. The full form of VLSI is _____
a) Very Long Single Integration
c) Very Large Scale Integration
b) Very Least Scale Integration
d) Very Long Scale Integration

34. In FPGA, vertical and horizontal directions are separated by _____
a) A line
c) A strobe
b) A channel
d) A flip-flop

35. Applications of PLAs are _____
a) Registered PALs
c) PAL programming
b) Configurable PALs
d) All of the Mentioned

36. Which type of ADC is chosen for noisy environment?
a) Successive approximation ADC
c) Charge balancing ADC
b) Dual slope
d) All of the mentioned

37. Which among the following has long conversion time?
a) Servo converter
c) Flash converter
b) Dual ramp converter
d) None of the mentioned

38. At what condition error occurs in the servo tracking A/D Converter?
a) Slow change input
c) No change in input
b) Rapid change in input
d) All of the mentioned

39. The number of comparator required for flash type A/D converter
a) Triples for each added bit
b) Reduce by half for each added bit
c) Double for each added bit
d) Doubles exponentially for each added bit

40. The flash type A/D converters are called as
a) Parallel non-inverting A/D converter
b) Parallel counter A/D converter
c) Parallel inverting A/D converter
d) Parallel comparator A/D converter

41. What is the advantage of using flash type A/D converter?
a) High speed conversion
c) Nominal speed conversion
b) Low speed conversion
d) None of the mentioned

42. In a servo tracking A/D converter, the input voltage is greater than the DAC output signal at this condition

a) The counter count up
c) The counter back and forth
b) The counter count down
d) None of the mentioned