



Maratha Vidya Prasarak Samaj's

Rajarshi Shahu Maharaj Polytechnic, Nashik

Udoji Maratha Boarding Campus, Near Pumping Station, Gangapur Road, Nashik-13.

Affiliated to MSBTE Mumbai, Approved by AICTE New Delhi, DTE Mumbai & Govt. of Maharashtra, Mumbai.

*Subject: - Digital Techniques
& Microprocessor (22323)*



SYLLABUS

Chapter No.	Name of chapter	Marks
1	Number Systems, Digital Logic families and logic gates	16
2	Combinational Logic Circuits	14
3	Sequential Logic Circuits	12
4	Microprocessor: 8086 and modern microprocessors	12
5	Assembly Language Programming using 8086	16
Total Marks: -		70

BOARD THEORY

PAPER PATTERN

FOR DTM (22323)

Q.1		Attempt any FIVE	5*2=10
	a)	Define following- 1. Fan In 2. Noise Margin	
	b)	State the features of 8086 processor.	
	c)	Explain the concept of min term and max term.	
	d)	Choose the instruction for following operations- 1. To exchange the contents of two 16 bit numbers 2. To compare two numbers in AX & BX 3. To add two 16 bit numbers with carry 4. To find 1's complement of a number	
	e)	Differentiate between RISC & CISC processor	
	f)	Differentiate between combinational circuits & Sequential circuits	
	g)	Draw symbol & truth table of EX-OR and EX-NOR gates.	
Q.2		Attempt any THREE	3*4=12
	a)	Write the Boolean equation & Draw logic diagram for the logic that will have output as Y & inputs A, B, C. The logic performs following operation- 1. Y=1 when A=B=C=0	

		2. $Y=1$ when $A=C=1$ & $B=0$ 3. $Y=0$ for all other cases
	b)	Perform the subtraction using 2's complement method- $(83)_{10}-(67)_{10}$.
	c)	Explain how race around condition is overcome using master slave J-K flip- flop.
	d)	Convert the following expression into its canonical form- $Y=(A+B)(B+C)(A+C)$
Q.3		Attempt any THREE 3*4=12
	a)	Realize the following expression using Multiplexer- $Y=\sum m(1,4,6,8,11,14,15)$
	b)	Explain the following Assembler Directives- 1. DB 2. DW 3. ENDS 4. DUP
	c)	State the function of following pins of 8086 processor- 1. $\overline{\text{LOCK}}$ 2. ALE 3. INTA 4. HOLD
	d)	Convert the following numbers- 1. $(23)_{10}-(?)_2$ 2. $(314)_8-(?)_{10}$
Q.4		Attempt any FOUR 3*4=12
	a)	1. Minimize the expression using K-map $Y=\sum m(0,2,4,5,13,14,15)$
	b)	Design AND & OR gate using universal NAND gate
	c)	Explain the operation of positive edge triggered S-R flip-flop
	d)	Explain the following Addressing modes 1. Immediate 2. Register 3. Direct 4. Register Indirect



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	e)	Write down the excitation tables for D & T flip-flop																																			
Q.5		Attempt any TWO 2*6=12																																			
	a)	Design full adder using k-map and draw logic diagram																																			
	b)	Explain minimum mode configuration of 8086 processor & also explain the function of each control signals used.																																			
	c)	Write an ALP to add array of 10 data bytes & assume that result is greater than 16 bits.																																			
Q.6		Attempt any TWO 2*6=12																																			
	a)	Write an ALP to find smallest number in an array of 5 numbers. Also draw flowchart.																																			
	b)	Draw flag register format of 8086 & Describe the operation of each flag																																			
	c)	1. For the following circuit find out the values of output Y for the given inputs- <table border="1" style="margin-left: auto; margin-right: auto;"><thead><tr><th colspan="4">Inputs</th><th>Output</th></tr><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>Y</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td></td></tr><tr><td>.</td><td>.</td><td>.</td><td>.</td><td></td></tr><tr><td>.</td><td>.</td><td>.</td><td>.</td><td></td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td></td></tr></tbody></table>	Inputs				Output	A	B	C	D	Y	0	0	0	0		0	0	0	1			1	1	1	1	
Inputs				Output																																	
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CLASS TEST - I

PAPER PATTERN

COURSE: - Digital Techniques & Microprocessor (22323)

PROGRAMME: - Information Technology

Syllabus: -

Unit No.	Name of the Unit	Course Outcome (CO)
1	Number Systems, Digital Logic families and logic gates	CO-323.1
2	Combinational Logic Circuits	CO-323.2
3	Sequential Logic Circuits	CO-323.1

Q.1	Attempt any FOUR 4*2=8Marks	Course Outcome (CO)
a)	Convert following no into decimal- $(314)_8$.	CO-323.1
b)	Define noise margin & Fan in.	CO-323.1
c)	Draw symbols of AND, EX-OR gate.	CO-323.1
d)	Convert standard SOP expression into canonical SOP: $Y = A + BCD$	CO-323.2
e)	Draw K-Map for $Y = \sum m(0,1,2,4,5,6)$ and simplify	CO-323.2
f)	Draw one bit memory cell.	CO-323.3
Q.2	Attempt any THREE 3*4=12 Marks	
a)	Explain De-Morgan's Theorems.	CO-323.1
b)	Design half adder using K-Map.	CO-323.2
c)	Explain NAND as universal gate	CO-323.2
d)	Perform subtraction using 2's complement method- $(12)_{10} - (8)_{10}$.	CO-323.1
e)	Design 8:1 using 4:1 MUX	CO-323.2
f)	Implement using MUX: $Y = \pi M(1,5,9,10,11,15)$	CO-323.2



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CLASS TEST - II

PAPER PATTERN

COURSE: - Digital Techniques & Microprocessor (22323)

PROGRAMME: - Information Technology

Syllabus: -

Unit No.	Name of the Unit	Course Outcome (CO)
3	Sequential Logic Circuits	CO-323.3
4	Microprocessor: 8086 and modern microprocessors	CO-323.4
5	Assembly Language Programming using 8086	CO-323.5

		Course Outcome (CO)
Q.1	Attempt any FOUR 4*2=8Marks	
a)	Sequential Logic Circuits.	CO-323.3
b)	Microprocessor: 8086 and modern microprocessors	CO-323.4
c)	Assembly Language Programming using 8086	CO-323.5
d)	Microprocessor: 8086 and modern microprocessors.	CO-323.4
e)	Sequential Logic Circuits	CO-323.3
f)	Assembly Language Programming using 8086	CO-323.5
Q.2	Attempt any THREE 3*4=12 Marks	
a)	Assembly Language Programming using 8086	CO-323.5
b)	Sequential Logic Circuits	CO-323.3
c)	Microprocessor: 8086 and modern microprocessors	CO-323.4



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COURSE OUTCOME

(CO)

COURSE: - DIGITAL TECHNIQUES & MICROPROCESSOR (22323)

PROGRAMME: - Information Technology

CO. NO.	Course Outcome
CO-323.1	Test the Digital Systems, Logic Families & Logic Gates
CO-323.2	Construct Combinational Logic Circuit
CO-323.3	Construct Sequential Logic Circuit
CO-323.4	Use registers and instructions of 8086
CO-323.5	Develop assembly language program using 8086



1. Number Systems, Digital Logic families and logic gates

Position in Question Paper

Total Marks-16

Q.1. a) 2-Marks.

Q.1. g) 2-Marks.

Q.2. a) 4-Marks.

Q.2. b) 4-Marks.

Q.3. d) 4-Marks.

Q.4. b) 6-Marks.

Descriptive Question

- List one application of each of following:
 - Gray code
 - ASCII code
- Define the following term with respect the digital IC's:
 - Propogation delay
 - Fan in
 - Fan out
 - Power Dissipation
 - Noise Margin
 - Threshold Voltage.
- Convert the following numbers into Hexadecimal number.
 - $(10110111)_2 = (?)_{16}$
 - $(567)_8 = (?)_{16}$
- Perform the following subtraction using 1's compliment and 2's compliment $(1010\ 0101)_2 - (1110\ 1110)_2$.
- Describe the characteristics of digital IC's (Any four).
- Reduce the following boolean expression using laws of Boolean algebra and realize using basic logic gates.
 - $Y = (A + BC)(B + \underline{C}A)$
- State the names of universal logic gates and design basic gates using universal gates.
- State any two Boolean laws with expression.
- Define:
 - Bit
 - Nibble
- Convert following number into its equivalent Binary Number $(146.25)_{10}$.

11. Perform binary subtraction using 2's complement of the following:

a) $(63)_{10} - (20)_{10} = ?$

b) $(34)_{10} - (48)_{10} = ?$

12. Simplify the following Boolean expression

a) $Y = AB + ABC + \underline{A}B + \underline{A}\underline{B}C$

b) $Y = (A + B)(A + \underline{B})(\underline{A} + B)$.

13. Construct NOT, AND, OR, NOR gates using NAND gate.

14. State and prove De-Morgan's Theorems.

15. Refer given Fig. No. 1 and write the outputs for each of the following input:

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

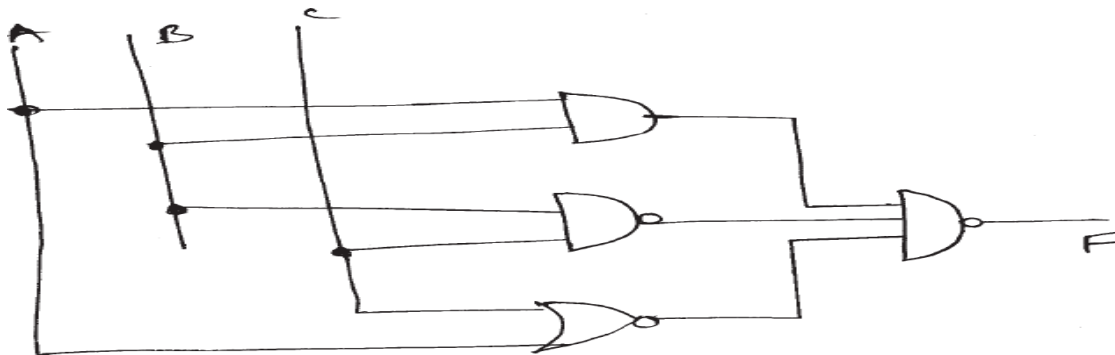


Fig. No. 1

16. Draw symbol and write truth table of EX-OR gate.

17. Convert following decimal to octal and Hexadecimal

a) $(297)_{10} = ()_8$

b) $(453)_{10} = ()_{16}$

18. Implement "OR" gate and "NOT" gate using "Universal NAND" gate. Write expressions for both.



MCQ Question

(Total number of Question=Marks*3=16*3=48)

Note: Correct answer is marked with **bold**.

- The given hexadecimal number $(1E.53)_{16}$ is equivalent to _____
a) $(35.684)_8$ c) $(34.340)_8$
b) **$(36.246)_8$** d) $(35.599)_8$
- The given hexadecimal number $(1E.53)_{16}$ is equivalent to _____
a) $(35.684)_8$ c) $(34.340)_8$
b) **$(36.246)_8$** d) $(35.599)_8$
- The octal equivalent of the decimal number $(417)_{10}$ is _____
a) **$(641)_8$** c) $(640)_8$
b) $(619)_8$ d) $(598)_8$
- Octal to binary conversion: $(24)_8 = ?$
a) $(111101)_2$ c) $(111100)_2$
b) **$(010100)_2$** d) $(101010)_2$
- Convert binary to octal: $(110110001010)_2 = ?$
a) $(5512)_8$ c) $(4532)_8$
b) **$(6612)_8$** d) $(6745)_8$
- What is the addition of the binary numbers 11011011010 and 010100101 ?
a) 0111001000 c) **1110111111**
b) 1100110110 d) 10011010011
- Perform binary subtraction: $101111 - 010101 = ?$
a) 100100 c) **011010**
b) 010101 d) 011001
- On multiplication of (10.10) and (01.01) , we get _____
a) 101.0010 c) **011.0010**
b) 0010.101 d) 110.0011
- Binary subtraction of $101101 - 001011 = ?$
a) **100010** c) 110101
b) 010110 d) 101100
- 1's complement of 1011101 is _____
a) 0101110 c) **0100010**
b) 1001101 d) 1100101
- On subtracting $(01010)_2$ from $(11110)_2$ using 1's complement, we get _____



- a) 01001
b) 11010
- c) 10101
d) **10100**
12. On subtracting $(001100)_2$ from $(101001)_2$ using 2's complement, we get _____
- a) 1101100
b) **011101**
- c) 11010101
d) 11010111
13. In boolean algebra, the OR operation is performed by which properties?
- a) Associative properties
b) Commutative properties
- c) Distributive properties
d) **All of the Mentioned**
14. According to boolean law: $A + 1 = ?$
- a) **1**
b) A
- c) 0
d) A'
15. DeMorgan's theorem states that _____
- a) **$(AB)' = A' + B'$**
b) $(A + B)' = A' * B$
- c) $A' + B' = A'B'$
d) $(AB)' = A' + B$
16. $(A + B)(A' * B') = ?$
- a) 1
b) **0**
- c) AB
d) AB'
17. Simplify $Y = AB' + (A' + B)C$.
- a) **$AB' + C$**
b) $AB + AC$
- c) $A'B + AC'$
d) $AB + A$
18. The code where all successive numbers differ from their preceding number by single bit is _____
- a) Alphanumeric Code
b) BCD
- c) Excess 3
d) **Gray**
19. The NOR gate output will be high if the two inputs are _____
- a) **00**
b) 01
- c) 10
d) 11
20. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
- a) **Venn Diagram**
b) Cycle Diagram
- c) Block diagram
d) Triangular Diagram
21. Each product term of a group, $w'.x.y'$ and $w.y$, represents the _____ in that group.
- a) Input
b) POS
- c) **Sum-of-Minterms**
d) Sum of Maxterms
22. Product-of-Sums expressions can be implemented using _____
- a) 2-level OR-AND logic circuits
b) 2-level NOR logic circuits



- c) 2-level XOR logic circuits
- d) **Both 2-level OR-AND and NOR logic circuits**

23. Reflected binary code is also known as _____

- a) BCD code
- b) Binary code
- c) ASCII code
- d) **Gray Code**

24. The binary representation of BCD number 00101001 (decimal 29) is _____

- a) **0011101**
- b) 0110101
- c) 1101001
- d) 0101011

25. A code converter is a logic circuit that _____

- a) Inverts the given input
- b) Converts into decimal number
- c) **Converts data of one type into another type**
- d) Converts to octal

26. The excess-3 code for 597 is given by _____

- a) **100011001010**
- b) 100010100111
- c) 010110010111
- d) 010110101101

27. When numbers, letters or words are represented by a special group of symbols, this process is called _____

- a) Decoding
- b) **Encoding**
- c) Digitizing
- d) Inverting

28. Which of the following statements apply to CMOS devices?

- a) The devices should not be inserted into circuits with the power on
- b) All tools, test equipment and metal workbenches should be tied to earth ground
- c) The devices should be stored and shipped in antistatic tubes or conductive foam
- d) **All of the Mentioned**

29. Integrated circuits are classified as _____

- a) Large, Small and Medium
- b) Very Large, Small and Linear
- c) **Linear and Digital**
- d) Non-Linear and Digital

30. Which logic is the fastest of all the logic families?

- a) TTL
- b) **ECL**
- c) HTL
- d) DTL

31. Sometimes ECL can also be named as _____

- a) EEL
- b) CEL
- c) **CML**
- d) CCL

Explanation: ECL (Emitter Coupled Logic) can also be named as CML (Collector Mode Logic).

32. In an ECL the output is taken from _____



- a) Emitter
b) Base
- c) **Collector**
d) Junction of emitter and base
33. The ECL behaves as _____
a) NOT gate
b) **NOR gate**
c) NAND gate
d) AND gate
34. ECL's major disadvantage is that _____
a) **It requires more power**
b) It's fanout capability is high
c) It creates more noise
d) It is slow
35. Transistor-transistor logic (TTL) is a class of digital circuits built from _____
a) JFET only
b) Bipolar junction transistors (BJT)
c) Resistors
d) **Bipolar junction transistors (BJT) and resistors**
36. TTL is called transistor-transistor logic because both the logic gating function and the amplifying function are performed by _____
a) Resistors
b) **Bipolar junction transistors**
c) One transistor
d) Resistors and transistors respectively
37. TTL inputs are the emitters of a _____
a) Transistor-transistor logic
b) **Multiple-emitter transistor**
c) Resistor-transistor logic
d) Diode-transistor logic
38. Standard TTL circuits operate with a ___ volt power supply.
a) 2
b) 4
c) **5**
d) 3
39. CMOS refers to _____
a) Continuous Metal Oxide Semiconductor
b) **Complementary Metal Oxide Semiconductor**
c) Centred Metal Oxide Semiconductor
d) Concrete Metal Oxide Semiconductor
40. Propagation delay is defined as _____
a) **the time taken for the output of a gate to change after the inputs have changed**
b) the time taken for the input of a gate to change after the outputs have changed
c) the time taken for the input of a gate to change after the intermediates have changed



- d) the time taken for the output of a gate to change after the intermediates have changed
41. Power Dissipation in DIC is expressed in _____
- a) Watts or kilowatts
b) **Milliwatts or nanowatts**
c) DB
d) Mdb
42. Fan-in is defined as _____
- a) the number of outputs 0connected to gate without any degradation in the voltage levels
b) **the number of inputs connected to gate without any degradation in the voltage levels**
c) the number of outputs connected to gate with degradation in the voltage levels
d) the number of inputs connected to gate with degradation in the voltage levels
43. The maximum noise voltage that may appear at the input of a logic gate without changing the logical state of its output is termed as _____
- a) Noise Margin
b) **Noise Immunity**
c) White Noise
d) Signal to Noise Ratio
44. Fan-in and Fan-out are the characteristics of _____
- a) Registers
b) **Logic families**
c) Sequential Circuits
d) Combinational Circuits
45. Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?
- a) OR gates only
b) AND gates and NOT gates
c) **AND gates, OR gates, and NOT gates**
d) OR gates and NOT gates
46. A single transistor can be used to build which of the following digital logic gates?
- a) AND gates
b) OR gates
c) **NOT gates**
d) NAND gates
47. Which input values will cause an AND logic gate to produce a HIGH output?
- a) At least one input is HIGH
b) At least one input is LOW
c) **All inputs are HIGH**
d) All inputs are LOW
48. The code where all successive numbers differ from their preceding number by single bit is _____
- a) Alphanumeric Code
b) BCD
c) Excess 3
d) **Gray**

2. Combinational Logic Circuit

Position in Question Paper

Total Marks-14

Q.1. c) 2-Marks.

Q.2. d) 4-Marks.

Q.3. a) 4-Marks.

Q.4. a) 4-Marks.

Q.4. c) 4-Marks.

Q.5. a) 6-Marks.

Descriptive Question

- Design half adder using K-map and realize it using basic gate.
- Define Minterm and Maxterm.
- Draw three variable K-map format.
- Simplify the given K-map using standard form and realize the circuit using gates. Refer Fig. No. 2.

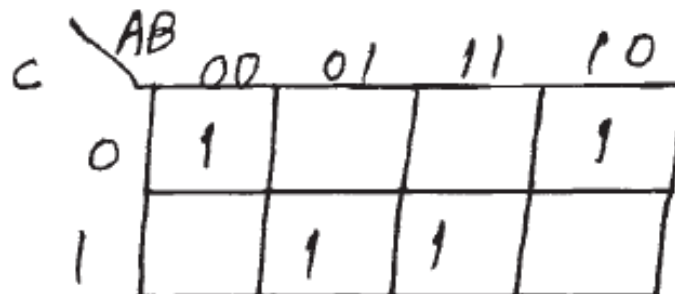


Fig. No. 2

- Minimize the four variable logic function using K-map.
 - $f(A,B,C,D) \Sigma m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$
- Describe the construction of half adder using K-map
- Minimize the following function using K-map. $F = \Sigma m (0,1,2,3,11,12,14,15)$.
- Define terms "Minterm" and "Maxterm" with proper example of each.
- Draw 16:1 multiplexer using 4:1 multiplexers "ONLY" with proper labels.
- Convert the given minterm into standard POS form

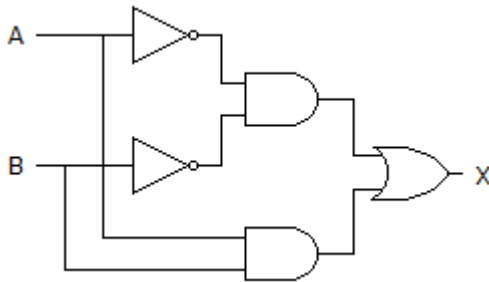
$$Y(A,B,CD) = (\underline{A} \cdot BC) + (B \cdot \underline{C} D) + (\underline{A} B)$$

MCQ Question

(Total number of Question=Marks*3=14*3=42)

Note: Correct answer is marked with **bold**

- Which of the following logic expressions represents the logic diagram shown?



- $X=AB'+A'B$
 - $X=(AB)'+AB$
 - $X=(AB)^'+A'B'$
 - $X=A'B'+AB$
- Which of the following combinations of logic gates can decode binary 1101?
 - One 4-input AND gate
 - One 4-input AND gate, one inverter**
 - One 4-input AND gate, one OR gate
 - One 4-input NAND gate, one inverter
 - What is the indication of a short to ground in the output of a driving gate?
 - Only the output of the defective gate is affected
 - There is a signal loss to all load gates**
 - The node may be stuck in either the HIGH or the LOW state
 - The affected node will be stuck in the HIGH state
 - What is a multiplexer?
 - It is a type of decoder which decodes several inputs and gives one output
 - A multiplexer is a device which converts many signals into one**
 - It takes one input and results into many output
 - It is a type of encoder which decodes several inputs and gives one output
 - Which is the major functioning responsibility of the multiplexing combinational circuit?
 - Decoding the binary information
 - Generation of all minterms in an output function with OR-gate
 - Generation of selected path between multiple sources and a single destination**
 - Encoding of binary information
 - In a multiplexer, the selection of a particular input line is controlled by _____
 - Data controller
 - Selected lines**



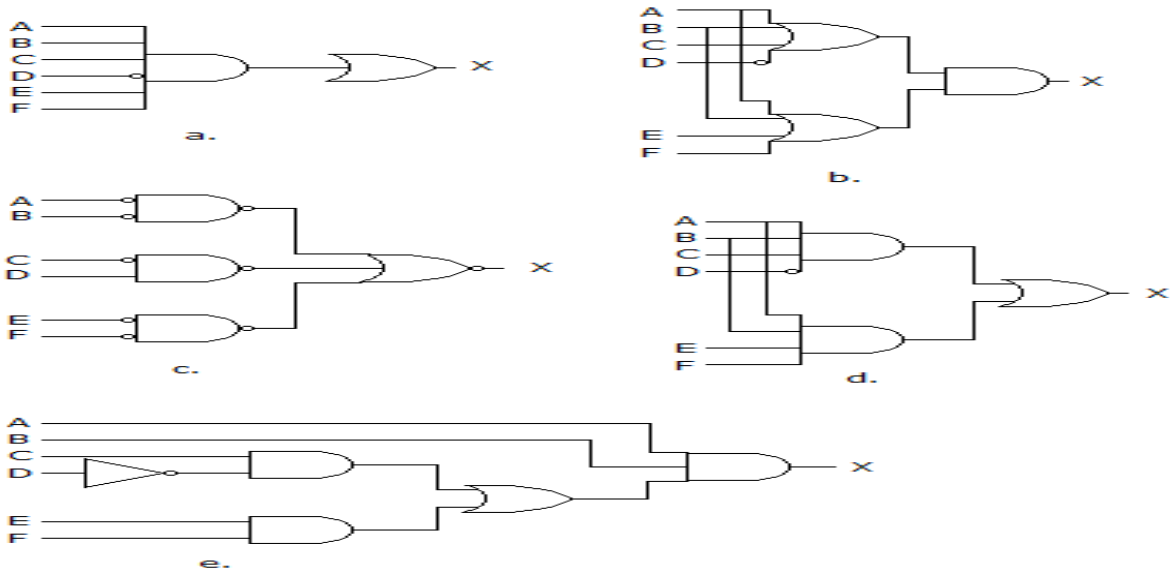
- c) Logic gates
d) Both data controller and selected lines
7. If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
- a) 2
b) **m**
c) n
d) 2^n
8. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
- a) 3
b) 4
c) **2**
d) 5
9. The enable input is also known as _____
- a) Select input
b) Decoded input
c) **Strobe**
d) Sink
10. 4 to 1 MUX would have _____
- a) 2 inputs
b) 3 inputs
c) **4 inputs**
d) 5 inputs
11. A combinational circuit that selects one from many inputs are _____
- a) Encoder
b) Decoder
c) Demultiplexer
d) **Multiplexer**
12. If enable input is high then the multiplexer is _____
- a) Enable
b) **Disable**
c) Saturation
d) High Impedance
13. The word demultiplex means _____
- a) One into many
b) Many into one
c) Distributor
d) **One into many as well as Distributor**
14. In a multiplexer the output depends on its _____
- a) Data inputs
b) **Select inputs**
c) Select outputs
d) Enable pin
15. In 1-to-4 demultiplexer, how many select lines are required?
- a) **2**
b) 3
c) 4
d) 5
16. How many AND gates are required for a 1-to-8 multiplexer?
- a) 2
b) 6
c) **8**
d) 5
17. Most demultiplexers facilitate which type of conversion?
- a) Decimal-to-hexadecimal
b) **Single input, multiple outputs**
c) AC to DC
d) Odd parity to even parity

18. The basic building blocks of the arithmetic unit in digital computers are _____
- a) Subtractors
 - b) Adders**
 - c) Multiplexer
 - d) Comparator
19. The design of an ALU is based on _____
- a) Sequential logic
 - b) Combinational logic**
 - c) Multiplexing
 - d) De-Multiplexing
20. 3 bits full adder contains _____
- a) 3 combinational inputs
 - b) 4 combinational inputs
 - c) 6 combinational inputs
 - d) 8 combinational inputs**
21. Which of the following circuit can be used as parallel to serial converter?
- a) Multiplexer**
 - b) Demultiplexer
 - c) Decoder
 - d) Digital counter
22. The Boolean expression $Y = (AB)'$ is logically equivalent to what single gate?
- a) NAND**
 - b) NOR
 - c) AND
 - d) OR
23. The systematic reduction of logic circuits is accomplished by _____
- a) Symbolic reduction
 - b) TTL logic
 - c) Using Boolean algebra**
 - d) Using a truth table
24. Each "1" entry in a K-map square represents _____
- a) A HIGH for each input truth table condition that produces a HIGH output**
 - b) A HIGH output on the truth table for all LOW input combinations
 - c) A LOW output for all possible HIGH input conditions
 - d) A DON'T CARE condition for all possible input truth table combinations
25. Each "0" entry in a K-map square represents _____
- a) A HIGH for each input truth table condition that produces a HIGH output**
 - b) A HIGH output on the truth table for all LOW input combinations
 - c) A LOW output for all possible HIGH input conditions
 - d) A DON'T CARE condition for all possible input truth table combinations
26. Which of the following expressions is in the product-of-sums form?
- a) $(A + B)(C + D)$**
 - b) $(AB)(CD)$
 - c) $AB(CD)$
 - d) $AB + CD$
27. If A, B and C are the inputs of a full adder then the sum is given by _____
- a) A AND B AND C
 - b) A OR B AND C
 - c) **A XOR B XOR C**
 - d) A OR B OR C
28. Half-adders have a major limitation in that they cannot _____
- a) Accept a carry bit from a present stage
 - b) Accept a carry bit from a next stage



- c) **Accept a carry bit from a previous stage**
d) Accept a carry bit from the following stages
29. How many outputs are required for the implementation of a subtractor?
a) 1
b) **2**
c) 3
d) 4
30. Which of the following is an important feature of the sum-of-products form of expressions?
a) **All logic circuits are reduced to nothing more than simple AND and OR operations**
b) The delay times are greatly reduced over other forms
c) No signal must pass through more than two gates, not including inverters
d) The maximum number of gates that any signal must pass through is reduced by a factor of two
31. All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) **NAND and NOR operations**
32. Without any additional circuitry an 8:1 MUX can be used to obtain _____
a) Some but not all Boolean functions of 3 variables
b) All function of 3 variables but none of 4 variables
c) All functions of 3 variables and some but not all of 4 variables
d) **All functions of 4 variables**
33. The inputs/outputs of an analog multiplexer/demultiplexer are _____
a) **Bidirectional**
b) Unidirectional
c) Even parity
d) Binary-coded decimal
34. Why is a demultiplexer called a data distributor?
a) **The input will be distributed to one of the outputs**
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input gives single output
35. In 1-to-4 demultiplexer, how many select lines are required?
a) **2**
b) 3
c) 4
d) 5
36. How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) **3**
c) 4
d) 5

37. What is the major difference between half-adders and full-adders?
- Full-adders are made up of two half-adders
 - Full adders can handle double-digit numbers
 - Full adders have a carry input capability**
 - Half adders can handle only single-digit numbers
38. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



- a
 - b
 - c
 - d**
40. Let the input of a subtractor is A and B then what the output will be if $A = B$?
- 0**
 - 1
 - A
 - B
41. Let A and B is the input of a subtractor then the borrow will be _____
- A AND B'
 - A' AND B**
 - A OR B
 - A AND B
42. The full subtractor can be implemented using _____
- Two XOR and an OR gates
 - Two half subtractors and an OR gate**
 - Two multiplexers and an AND gate
 - Two comparators and an AND gate



3. Sequential Logic Circuit

Position in Question Paper

Total Marks-12

Q.1. f) 2-Marks.

Q.2. c) 4-Marks.

Q.4. c) 6-Marks.

Descriptive Question

1. Differentiate between combinational circuits & Sequential circuits
2. Explain the operation of positive edge triggered S-R flip-flop
3. Explain how race around condition is overcome using master slave J-K flip-flop
4. Write excitation tables for D & T flip-flop.
5. Explain RS latch
6. What is triggering? Also explain types of triggering.
7. What is clock signal?
8. Draw symbol truth table of SR & JK flip-flop.
9. State four applications of flip-flop.
10. Describe race-around condition in JK flip flop and suggest ways to overcome it
11. Draw symbol and truth table of D and T flip flop. State their applications.
12. Describe the principle of working of JK FF and draw its circuit diagram and truth table.
13. Differentiate between sequential and combinational logic circuits. (Any four points)
14. Draw symbol of JK flipflop and write its truth table.
15. Draw waves for positive and negative edge triggering with proper labeling. Identify two situations where these triggering can be used?
16. Draw symbol and write truth table for the following flip flop and give one application of each.
 - a) Clocked R-S flipflop
 - b) T - Flip flop



MCQ Question

(Total number of Question=Marks*3=12*3=36)

Note: Correct answer is marked with **bold**

- Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
 - Low input voltages
 - Synchronous operation
 - Gate impedance
 - Cross coupling**
- The truth table for an S-R flip-flop has how many VALID entries?
 - 1
 - 2
 - 3**
 - 4
- When both inputs of a J-K flip-flop cycle, the output will _____
 - Be invalid
 - Change
 - Not change**
 - Toggle
- The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called _____
 - Combinational circuits
 - Sequential circuits**
 - Latches
 - Flip-flops
- The sequential circuit is also called _____
 - Flip-flop
 - Latch**
 - Strobe
 - Adder
- The output of latches will remain in set/reset until _____
 - The trigger pulse is given to change the state**
 - Any pulse given to go into previous state
 - They don't get any pulse more
 - The pulse is edge-triggered
- What is an ambiguous condition in a NAND based S'-R' latch?
 - $S'=0, R'=1$
 - $S'=1, R'=0$
 - $S'=1, R'=1$
 - $S'=0, R'=0$**
- One major difference between a NAND based S'-R' latch & a NOR based S-R latch is _____
 - The inputs of NOR latch are 0 but 1 for NAND latch**
 - The inputs of NOR latch are 1 but 0 for NAND latch
 - The output of NAND latch becomes set if $S'=0$ & $R'=1$ and vice versa for NOR latch
 - The output of NOR latch is 1 but 0 for NAND latch

9. The difference between a flip-flop & latch is _____
- Both are same
 - Flip-flop consist of an extra output
 - Latches has one input but flip-flop has two**
 - Latch has two inputs but flip-flop has one
10. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
- The clock pulse is LOW
 - The clock pulse is HIGH
 - The clock pulse transitions from LOW to HIGH**
 - The clock pulse transitions from HIGH to LOW
11. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the _____
- Edge-detection circuit**
 - NOR latch
 - NAND latch
 - Pulse-steering circuit
12. Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs?
- Gated JK-latch
 - Gated SR-latch
 - Gated T-latch
 - Gated D-latch**
13. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
- Two AND gates**
 - Two NAND gates
 - Two NOT gates
 - Two OR gates
14. In J-K flip-flop, "no change" condition appears when _____
- $J = 1, K = 1$
 - $J = 1, K = 0$
 - $J = 0, K = 1$
 - $J = 0, K = 0$**
15. On a J-K flip-flop, when is the flip-flop in a hold condition?
- $J = 0, K = 0$**
 - $J = 1, K = 0$
 - $J = 0, K = 1$
 - $J = 1, K = 1$
16. Four J-K flip-flops are cascaded with their J-K inputs tied HIGH. If the input frequency (f_{in}) to the first flip-flop is 32 kHz, the output frequency (f_{out}) is _____
- 1 kHz
 - 2 kHz**
 - 4 kHz
 - 16 kHz
17. In D flip-flop, D stands for _____
- Distant
 - Data**
 - Desired
 - Delay
18. In D flip-flop, if clock input is HIGH & $D=1$, then output is _____
- 0**
 - 1
 - Forbidden
 - Toggle

19. Which of the following is correct for a D latch?
- a) The output toggles if one of the inputs is held HIGH
 - b) Q output follows the input D when the enable is HIGH**
 - c) Only one of the inputs can be HIGH at a time
 - d) The output complement follows the input when enabled
20. A positive edge-triggered D flip-flop will store a 1 when _____
- a) The D input is HIGH and the clock transitions from HIGH to LOW
 - b) The D input is HIGH and the clock transitions from LOW to HIGH**
 - c) The D input is HIGH and the clock is LOW
 - d) The D input is HIGH and the clock is HIGH
21. The characteristic equation of D-flip-flop implies that _____
- a) The next state is dependent on previous state
 - b) The next state is dependent on present state
 - c) The next state is independent of previous state
 - d) The next state is independent of present state**
22. The asynchronous input can be used to set the flip-flop to the _____
- a) 1 state
 - b) 0 state
 - c) either 1 or 0 state**
 - d) forbidden State
23. Master slave flip flop is also referred to as?
- a) Level triggered flip flop
 - b) Pulse triggered flip flop**
 - c) Edge triggered flip flop
 - d) Edge-Level triggered flip flop
24. S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____
- a) OR Gate
 - b) AND Gate
 - c) Inverter**
 - d) Full Adder
25. Which of the following flip-flops is free from the race around the problem?
- a) T flip-flop**
 - b) SR flip-flop
 - c) Master-Slave Flip-flop
 - d) D flip-flop
26. How many types of triggering takes place in a flip flops?
- a) 3**
 - b) 2
 - c) 4
 - d) 5
27. In a J-K flip-flop, if $J=K$ the resulting flip-flop is referred to as _____
- a) D flip-flop
 - b) S-R flip-flop
 - c) T flip-flop**
 - d) S-K flip-flop
28. The only difference between a combinational circuit and a flip-flop is that _____
- a) The flip-flop requires previous state
 - b) The flip-flop requires next state
 - c) The flip-flop requires a clock pulse**
 - d) The flip-flop depends on the past as well as present states



29. The flip-flop is only activated by _____
- a) Positive edge trigger
 - b) Negative edge trigger
 - c) Either positive or Negative edge trigger**
 - d) Sinusoidal trigger
30. Both the J-K & the T flip-flop are derived from the basic _____
- a) S-R flip-flop
 - b) S-R latch**
 - c) D latch
 - d) D flip-flop
31. The flip-flops which has not any invalid states are _____
- a) S-R, J-K, D
 - b) S-R, J-K, T
 - c) J-K, D, S-R
 - d) J-K, D, T**
32. What does the triangle on the clock input of a J-K flip-flop mean?
- a) Level enabled
 - b) Edge triggered**
 - c) Both Level enabled & Edge triggered
 - d) Level triggered
33. What does the direct line on the clock input of a J-K flip-flop mean?
- a) Level enabled
 - b) Positive edge triggered
 - c) negative edge triggered
 - d) Level triggered**
34. On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
- a) The clock pulse is LOW
 - b) The clock pulse is HIGH
 - c) The clock pulse transitions from LOW to HIGH**
 - d) The clock pulse transitions from HIGH to LOW
35. In a NAND based S'-R' latch, if S'=1 & R'=1 then the state of the latch is _____
- a) No change**
 - b) Set
 - c) Reset
 - d) Forbidden
36. The characteristic equation of S-R latch is _____
- a) $Q(n+1) = (S + Q(n))R'$**
 - b) $Q(n+1) = SR + Q(n)R$
 - c) $Q(n+1) = S'R + Q(n)R$
 - d) $Q(n+1) = S'R + Q'(n)R$



4. Microprocessor 8086 and Modern Microprocessors

Position in Question Paper

Total Marks-12

Q.1. e) 2-Marks.

Q.3. c) 4-Marks.

Q.5. b) 4-Marks

Q.6. b) 6-Marks.

Descriptive Question

1. List features of 8086 microprocessor.
2. Describe the use of flag register and segment registers in 8086.
3. Differentiate between CISC and RISC and justify use of each of them in practice.
4. Describe the concept of pipelining and process of physical address generation in 8086 microprocessor.
5. State importance of pipelining in 8086 microprocessor
6. Draw minimum mode configuration of 8086 and explain the function of any four control signals.
7. Draw 8086 architecture block diagram and state the functions of EV and B/V.
8. State importance of pipelining in 8086 microprocessor.
9. Explain the concept of pipelining.
10. Define the following terms - (a) Physical Address (b) Effective Address
 - a) Differentiate between RISC and CISC processor (Three point)
 - b) Compare 8086 and 80586 (Pentium) (3 points)
11. Draw minimum mode configuration of 8086 and explain the function of each block.
12. Draw architectural block diagram of 8086 microprocessor and describe the function of each block.



MCQ Question

(Total number of Question=Marks*3=12*3=36)

Note: Correct answer is marked with **bold**

- If an interrupt is generated from outside the processor then it is an
 - internal interrupt
 - external interrupt**
 - interrupt
 - none of the mentioned
- Example of an external interrupt is
 - divide by zero interrupt
 - keyboard interrupt**
 - overflow interrupt
 - type2 interrupt
- The interrupt request that is independent of IF flag is
 - NMI
 - TRAP
 - Divide by zero
 - All of the mentioned**
- The type of the interrupt may be passed to the interrupt structure of CPU from
 - interrupt service routine
 - stack
 - interrupt controller**
 - none of the mentioned
- After every response to the single step interrupt the flag that is cleared is
 - IF (Interrupt Flag)
 - TF (Trap Flag)**
 - OF (Overflow Flag)
 - None of the mentioned
- When the CPU executes IRET,
 - contents of IP and CS are retrieved**
 - the control transfers from ISR to main program
 - clears the trap flag
 - clears the interrupt flag
- The interrupt for which the processor has the highest priority among all the external interrupts is
 - keyboard interrupt
 - TRAP
 - NMI**
 - INT
- In case of string instructions, the NMI interrupt will be served only after
 - initialisation of string
 - execution of some part of the string
 - complete string is manipulated**
 - the occurrence of the interrupt
- The INTR signal can be masked by resetting the
 - TRAP flag
 - INTERRUPT flag**
 - MASK flag
 - DIRECTION flag
- The disadvantage of CISC design processors is
 - low burden on compiler developers



- b) wide availability of existing software
c) **complex in nature**
d) none
11. The RISC architecture is preferred to CISC because RISC architecture has
a) simplicity
b) efficiency
c) high speed
d) **all of the mentioned**
12. The feature of RISC that is not present in CISC is
a) branch prediction
b) pipelining
c) **branch prediction and pipelining**
d) none
13. Which of the following processor belongs to hybrid RISC-CISC architecture?
a) Intel Pentium III
b) Intel Itanium 64
c) AMD's X86-64
d) **All of the mentioned**
14. The additional functionality that can be placed on the same chip of RISC is
a) Memory management units
b) Floating point units
c) **Memory management and floating point arithmetic units**
d) RAM, ROM
15. The number of CPIs (Clock Per Instruction) for an instruction of RISC processors is
a) 0
b) **1**
c) 2
d) 3
16. Which of the following is true about register windowing?
a) **chips expose 32 registers to programmer**
b) puts demands on multiplexers
c) puts enormous demands on register ports
d) all of the mentioned
17. The disadvantage of register windowing is
a) high speed
b) puts demands on multiplexers/register ports
c) consumes less cycles
d) **doesn't handle overflow/underflow**
18. 8086 has ___ address bus.
a) 16-bit
b) 18-bit
c) **20-bit**
d) 24-bit
19. Which flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0?
a) Binary bit
b) **Zero flag**
c) Sign flag
d) Overflow flag
20. It is used to write the data into the memory or the output device depending on the status of M/IO signal.



- a) IR
b) HLDA
21. The different ways in which a source operand is denoted in an instruction is known as
a) Instruction Set
b) Interrupts
c) 8086 Configuration
d) Addressing Modes
22. 8086 can access up to?
a) 512KB
b) 1Mb
c) 2Mb
d) 256KB
23. In order to implement complex instructions, CISC architectures use
a) macroprogramming
b) hardware
c) microprogramming
d) none
24. The stack pointer register contains
a) address of the stack segment
b) pointer address of the stack segment
c) offset of address of stack segment
d) data present in the stack segment
25. The stack segment register contains
a) address of the stack segment
b) base address of the stack segment
c) pointer address of the stack segment
d) data in the stack segment
26. In the instruction, ASSUME CS : CODE, DS : DATA, SS : STACK the ASSUME directive directs to the assembler the
a) address of the stack segment
b) pointer address of the stack segment
c) name of the stack segment
d) name of the stack, code and data segments
27. 8086 does not support
a) Arithmetic operations
b) logical operations
c) BCD operations
d) Direct BCD packed multiplication
28. For 8086 microprocessor, the stack segment may have a memory block of a maximum of
a) 32K bytes
b) 64K bytes
c) 16K bytes
d) NONE
29. When a stack segment is initialised then
a) SS and SP are initialised
b) only SS is initialised
c) only SP is initialised
d) SS and SP need not be initialized



30. The number of instructions actually executed by the microprocessor depends on the
- a) stack
 - b) loop count**
 - c) program counter
 - d) time duration
31. The feature of Pentium 4 is
- a) works based on NetBurst microarchitecture
 - b) clock speed ranges from 1.4GHz to 1.7GHz
 - c) has hyper-pipelined technology
 - d) all of the mentioned**
32. The instruction that is not possible among the following is
- a) MOV AX, BX
 - b) MOV AX, [BX].
 - c) MOV 55H, BL**
 - d) MOV AL, 55H
33. NMI stands for
- a) nonmaskable interrupt**
 - b) nonmultiple interrupt
 - c) nonmovable interrupt
 - d) none of the mentioned
34. The INTR interrupt may be
- a) maskable**
 - b) nonmaskable
 - c) maskable and nonmaskable
 - d) none of the mentioned
35. Example of an external interrupt is
- a) divide by zero interrupt
 - b) keyboard interrupt**
 - c) overflow interrupt
 - d) type2 interrupt
36. Example of an internal interrupt is
- a) divide by zero interrupt
 - b) overflow interrupt
 - c) interrupt due to INT
 - d) all of the mentioned**



5. Assembly Language Programming using 8086

Position in Question Paper

Total Marks-16

Q.1. d) 2-Marks.

Q.3. b) 4-Marks.

Q.5. c) 6-Marks.

Q.6. a) 6-Marks.

Descriptive Question

1. Give example of any two types of addressing mode of 8086.
2. List any four addressing modes and give one example of each.
3. List the addressing modes of 8086 and describe them with an example.
4. Write an assembly language program to arrange any array of 10 bytes in ascending order. Draw flowchart for the same.
5. Write an assembly language program to transfer block of 10 numbers from one memory location to another. (Assume suitable data.)
6. Write an assembly language program to find the sum of series of ten numbers stored in memory. (Assume suitable data.)
7. Write an assembly language program to find the factorial of a number using looping process.
8. Describe the use of shift and rotate instructions as well as string instructions with the help of one relevant examples of each.
9. Choose instruction for following situations:
 - a) Addition of 16bit Hex. No with carry
 - b) Division of 8bit No.
 - c) Rotate content of BL by 4 bit.
 - d) Perform logical AND operation of AX and BX.
10. Explain following instructions for 8 bit and 16bit data.
 - a) PUSH
 - b) DAA
 - c) IDIV
 - d) XOR
11. Suggest "Two instruction" for each of the following addressing modes.
 - a) Register Addressing Mode
 - b) Direct Addressing Mode

- c) Based Indexed Addressing Mode
 - d) Immediate Addressing Mode
12. Write algorithm and 8086 assembly language program to find average salary of five employees of "SILICON Systems" Assume 4digit salary of each employee. Also - write output.
13. Write an assembly language program to find the largest number from an array of a 10 numbers. Assume suitable data.
14. Interpret the given program and specify the output for the following situation.
- a) MOV AX, 34F9H
 - b) MOV BX, 3A69H.
 - c) Masking of lower nibble of AX.
 - d) Rotate right through carry contents of BX by 4 positions.
 - e) Shift left contents of BX by 6 positions.
 - f) XOR AX, BX
15. Write an assembly language program with algorithm for finding smallest number from the array of 10 numbers (Assume suitable data).
16. Choose instruction for following situations:
- a) Addition of 16 bit Hex. No with carry
 - b) Division of 8 bit No.
 - c) Rotate content of BL by 4 bit.
 - d) Perform logical AND operation of AX and BX .
17. Write an ALP to find smallest number in an array of 5 numbers.
18. Write an ALP to add array of 10 data bytes & assume that result is greater than 16 bits.
19. Write an ALP to multiply two 16 bit numbers and assume that result is greater than 16 bit.
20. Write an ALP to find out whether the number is even or odd.
21. Write an ALP to find out whether the number is positive or negative.



MCQ Question

(Total number of Question=Marks*3=16*3=48)

Note: Correct answer is marked with **bold**

- The instruction, MOV AX, 0005H belongs to the address mode
 - register
 - direct
 - immediate**
 - register relative
- The instruction, MOV AX, [2500H] is an example of
 - immediate addressing mode
 - direct addressing mode**
 - indirect addressing mode
 - register addressing mode
- If the offset of the operand is stored in one of the index registers, then it is
 - based indexed addressing mode
 - relative based indexed addressing mode
 - indexed addressing mode**
 - none of the mentioned
- If the offset of the operand is stored in one of the index registers, then it is
 - based indexed addressing mode
 - relative based indexed addressing mode
 - indexed addressing mode**
 - none of the mentioned
- The contents of a base register are added to the contents of index register in
 - indexed addressing mode
 - based indexed addressing mode
 - relative based indexed addressing mode
 - based indexed and relative based indexed addressing mode**
- The instruction, JMP 5000H:2000H; is an example of
 - intra-segment direct mode
 - intra-segment indirect mode
 - inter-segment direct mode**
 - inter-segment indirect mode
- The instruction that is used to transfer the data from source operand to destination operand is
 - data copy/transfer instruction
 - branch instruction
 - arithmetic/logical instruction
 - string instruction**
- The instructions that involve various string manipulation operations are
 - branch instructions
 - flag manipulation instructions
 - shift and rotate instructions
 - string instructions**
- Which of the following instruction is not valid?
 - MOV AX, BX
 - MOV DS, 5000H**
 - MOV AX, 5000H
 - PUSH AX



10. In POP instruction, after each execution of the instruction, the stack pointer is
- a) incremented by 1
 - b) decremented by 1
 - c) **incremented by 2**
 - d) decremented by 2
11. The instructions that are used for reading an input port and writing an output port respectively are
- a) MOV, XCHG
 - b) MOV, IN
 - c) IN, MOV
 - d) **IN, OUT**
12. The instruction that is used for finding out the codes in case of code conversion problems is
- a) XCHG
 - b) **XLAT**
 - c) XOR
 - d) JCXZ
13. The instruction that pushes the flag register on to the stack is
- a) PUSH
 - b) POP
 - c) **PUSHF**
 - d) POPF
14. The instruction that loads the flag register completely from the word contents of the memory location is
- a) PUSH
 - b) POP
 - c) PUSHF
 - d) **POPF**
15. The instruction that adds immediate data/contents of the memory location specified in an instruction/register to the contents of another register/memory location is
- a) SUB
 - b) **ADD**
 - c) MUL
 - d) DIV
16. The instruction that supports addition when carry exists is
- a) ADD
 - b) **ADC**
 - c) ADD & ADC
 - d) None of the mentioned
17. The mnemonic that is placed before the arithmetic operation is performed is
- a) AAA
 - b) AAS
 - c) AAM
 - d) **AAD**
18. The instruction that is used as prefix to an instruction to execute it repeatedly until the CX register becomes zero is
- a) SCAS
 - b) **REP**
 - c) CMPS
 - d) STOS
19. The instructions that are used to call a subroutine from the main program and return to the main program after execution of called function are
- a) CALL, JMP
 - b) JMP, IRET
 - c) **CALL, RET**
 - d) JMP, RET
20. Which instruction cannot force the 8086 processor out of 'halt' state?
- a) Interrupt request
 - b) Reset
 - c) Both interrupt request and reset
 - d) **Hold**
21. Which of the following is not a machine controlled instruction?



- a) HLT
b) **CLC**
- c) LOCK
d) ESC
22. If the data is present in a register and it is referred using the particular register, then it is
- a) direct addressing mode
b) **register addressing mode**
c) indexed addressing mode
d) immediate addressing mode
23. The contents of a base register are added to the contents of index register in
- a) indexed addressing mode
b) based indexed addressing mode
c) relative based indexed addressing mode
d) **based indexed and relative based indexed addressing mode**
24. Which of the following instruction is not valid?
- a) MOV AX, BX
b) **MOV DS, 5000H**
c) MOV AX, 5000H
d) PUSH AX
25. The instruction, MOV AX,[BX] is an example of
- a) direct addressing mode
b) register addressing mode
c) register relative addressing mode
d) **register indirect addressing mode**
26. Which of the following is not a data copy/transfer instruction?
- a) MOV
b) PUSH
c) **DAS**
d) POP
27. The instruction format 'register to register' has a length of
- a) **2 bytes**
b) 1 byte
c) 3 bytes
d) 4 bytes
28. The instructions which after execution transfer control to the next instruction in the sequence are called
- a) **Sequential control flow instructions**
b) control transfer instructions
c) Sequential control flow & control transfer instructions
d) none of the mentioned
29. The instruction "JUMP" belongs to
- a) sequential control flow instructions
b) control transfer instructions
c) branch instructions
d) **control transfer & branch instructions**
30. In PUSH instruction, after each execution of the instruction, the stack pointer is
- a) incremented by 1
b) decremented by 1
c) incremented by 2
d) **decremented by 2**



31. The instruction that pushes the contents of the specified register/memory location on to the stack is
- a) PUSHF
 - b) POPF
 - c) **PUSH**
 - d) POP
32. The instruction, MOV AX, 1234H is an example of
- a) register addressing mode
 - b) direct addressing mode
 - c) **immediate addressing mode**
 - d) based indexed addressing mode
33. _____ converts the programs written in assembly language into machine instructions.
- a) Machine compiler
 - b) Interpreter
 - c) **Assembler**
 - d) Converter
34. The instructions like MOV or ADD are called as _____
- a) **OP-Code**
 - b) Operators
 - c) Commands
 - d) None of the mentioned
35. The alternate way of writing the instruction, ADD #5,R1 is _____
- a) ADD [5],[R1];
 - b) **ADDI 5,R1;**
 - c) ADDIME 5,[R1];
 - d) There is no other way
36. Instructions which won't appear in the object program are called as _____
- a) Redundant instructions
 - b) Exceptions
 - c) Comments
 - d) **Assembler Directives**
37. _____ directive specifies the end of execution of a program
- a) End
 - b) **Return**
 - c) Stop
 - d) Terminate
38. The last statement of the source program should be _____
- a) Stop
 - b) Return
 - c) OP
 - d) **End**
39. The utility program used to bring the object code into memory for execution is _____
- a) **Loader**
 - b) Fetcher
 - c) Extractor
 - d) Linker
40. The assembler stores all the names and their corresponding values in _____
- a) Special purpose Register
 - b) **Symbol Table**
 - c) Value map Set
 - d) None of the mentioned
41. What is the content of Stack Pointer?
- a) Address of the current instruction
 - b) **Address of the top element of the stack**
 - c) Address of the next instruction
 - d) None of the mentioned



42. The instruction DEC N inform the assembler to
- a) **Decrement the content of N**
 - b) Decrement the data addressed by N
 - c) Convert signed decimal number to binary
 - d) None of the mentioned
43. If the interrupt is generated by the execution of an interrupt instruction then it is
- a) **internal interrupt**
 - b) external interrupt
 - c) interrupt-in-interrupt
 - d) none of the mentioned
44. The directive that marks the end of a logical segment is
- a) **ENDS**
 - b) END
 - c) ENDS & END
 - d) None of the mentioned
45. The directive that marks the starting of the logical segment is
- a) SEG
 - b) **SEGMENT**
 - c) SEG & SEGMENT
 - d) PROC
46. PUSH operation
- a) **decrements SP**
 - b) increments SP
 - c) decrements SS
 - d) increments SS
47. The number of PUSH instructions and POP instructions in a subroutine must be
- a) PUSH instructions must be greater than POP instructions
 - b) POP instructions must be greater than PUSH instructions
 - c) **Both must be equal**
 - d) Instructions may be any kind
48. The instruction, "INC" increases the contents of the specified register or memory location by
- a) 2
 - b) **1**
 - c) 0
 - d) 3